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Analog Test Board: Design and Operation

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1 Introduction

The Analog Test Board, or ATB, is a device designed to exercise and test current-mode analog circuits by providing up to 38 independently adjustable inputs and capturing up to six separate outputs. It is controlled through a parallel port such as the printer port found on most "PC clone" personal computers. The inputs are generated by Digital-Analog Converter chips (DACs) which receive 12-bit digital values from the controller; the outputs are converted to 12-bit digital values by Analog-Digital Converters (ADCs) whose results are polled by the controller. Test inputs to the analog circuit can be produced asynchronously or synchronously, after setting them up one at a time; output values can also be captured synchronously or asynchronously, then sent to the controller one by one. The inputs are current drains, and the test-circuit outputs are assumed to be also.

The ATB was originally designed and built by Charles Daffinger, who used it to test his LL9 and LL10 analog logic circuits. The original design was controlled through an RS-232 serial interface connected to a dedicated port on a VAX minicomputer; the 1200bps communication rate through the interface limited testing speed. The author re-engineered the interface to use a parallel port compatible with the printer port on an 80386-based desktop computer, providing communication speeds on the order of 10 kilobytes per second along with the convenience and flexibility of a dedicated personal computer for board control. In the process some hardware bugs were detected and repaired. This new configuration is used by the author to test the LL9 and KLLA analog logic circuits and others, including a digital implementation of the LL9/KLLA logic. (The LL9/KLLA logic is described in [MBD90] and [Mil91]. A KLLA test is described in [MM93].)

This technical report is organized in a bottom-up manner. Section 2 report describes the physical design of the ATB, with an eye toward maintaining it in operating condition. Section 3 describes the algorithms and programming used to control the ATB; an optional appendix[1] lists the software control-routine library and a general-purpose program presently used in

[1]The appendix is 64 pages of C-language source listing; it is available on request .

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testing operations on the board. The organization makes sense for maintaining the ATB (or building a new one); if a "user-level" programming guide is desired it may be helpful to skim the report backwards first for a more top-down view of the ATB's operation.

2 Physical Design

The ATB consists of a two-foot-by-three-foot platform with components mounted on its surface. The platform is a wooden frame covered by a grounded aluminum sheet; the sheet provides an electrical ground plane and partial shielding from electromagnetic interference. On top of the aluminum sheet are a number of functional units, wired on circuit prototyping boards which are attached to the sheet, and two small "perf board" circuit boards which hold the parallel-interface circuitry. Figure 3 is a schematic diagram of the ATB. The functional blocks in Figure 3 are cross-referenced to circuit diagrams in other figures by Figure 2.

2.1 Board Infrastructure

Power. The various circuits on the ATB require 5-volt power and ground to drive TTL-level chips, and +15 volts and -15 volts to power analog-digital converters and support circuitry. These voltages are supplied by an external voltage-regulated power supply, and distributed over the board. They can be tapped into from many points on the functional-unit prototyping boards. The power-supply ground is connected to the aluminum ground-plane, which is available everywhere on the board. In the circuit schematics, the +15V supply is identified as "+Red", referring to the color of the supply wire. "-Black" wires distribute -15V; +5V for the TTL logic is routed through white wires, and Ground connections use green wires.

Controlled Voltages. Figure 5 shows two op-amp based circuits which provide reference voltages for the test output-measuring circuits. The 5V reference is used in converting output current drains to voltage levels. The 10V reference is supplied to the ADC chips. One prototyping board holds both circuits, as well as the Clock circuit and part of the Sync circuit.

A 10V reference signal is also supplied to the DAC chips. One copy of the circuit in Figure 7 generates $V\text{ref}_0$ for the 18 DACs numbered **0x00** through **0x11**. Another copy generates $V\text{ref}_1$ for DACs **0x12** through **0x23**, **0x44** and **0x45**. The circuits are mounted on spare areas of the prototyping boards that hold devices **0x45** and **0x09**.

Clock. A Clock circuit is shown in Figure 6. A 10MHz clock signal is divided down to 78.125KHz, then supplied at 10V to the ADC chips and at 5V to the Sync circuit which generates *Convert.L*[2] signals for the ADC chips.

Signal Distribution. The various devices on the ATB receive data from the controller (via the Parallel Interface Board) over a 12-bit input data bus composed of red wires, referred to as ID11 through ID0. The output devices return data to the Parallel Interface Board over a 12-bit output data bus composed of blue wires, referred to as OD11 through OD0. Device addresses are decoded into individual enable signals (identified as *Write.L* in Figures 11, 9, 8, and 10) which are sent over distinct wires from the Address Decoder Board to each device.

2.2 Inputs

The ATB generates 36 current-drain signals as inputs to an analog circuit to be tested, plus two settable voltage signals intended as test-reference voltages. Each signal is produced by latching a 12-bit value S_{in} from the common input data bus into an Analog Devices AD1208 DAC, and issuing a *Write.L* signal to that DAC. The DAC also receives a reference voltage $V\text{ref}$ (supplied by one of the circuits in Figure 7), and emits an output current that drives a TL082 op amp[3] to produce a stable voltage given by $-\frac{S_{\text{in}}}{4095} \cdot V\text{ref}$. The DAC and op amp are shown in both Figures 9 and 8.

The DACs are double-buffered, and can be controlled either to convert S_{in} immediately or to wait until a separate *Xfer.L* signal is received. When

[2]The notation *signal.L* refers to a controlling signal which is logically true when its electrical value is 0V. This notation is described in [PW87]; IC schematics often write such signals in the form $\overline{signal}$.

[3]Both 47pF and 100pF feedback capacitors are used with the op amps; the exact value is not critical.

a DAC is addressed, the Address Decode Board converts the address into a *Write.L* signal which enables the appropriate DAC to latch a new S_{in}. The constant-voltage DACs (see below) are hardwired to convert S_{in} immediately. The current-drain DACs share a common *Xfer.L* signal; when they receive it (from device **0x40**, see §2.4.1) they all convert their new values simultaneously. This makes it possible to load distinct S_{in} values to each of the current-drain DACs, and then present them all to the test circuit at the same time. Alternatively, *Xfer.L* can be reissued after each DAC (or subset of DACs) is loaded, to convert new values as they are sent.

2.2.1 Current-Drain Signals

As seen in Figure 3, there are two banks of 18 signal-DAC functional units that drain selectable amounts of current. The units have hexadecimal addresses **0x00** through **0x11** and **0x12** through **0x23**. Each unit consists of the circuit depicted in Figure 9, built on (half of) a prototyping board. The DAC/op amp output voltage, described above, is inverted through a $100K\Omega$ resistor to a positive voltage by a second op amp.[3] The positive voltage controls a 2N5486 JFET transistor which acts as a current drain. It will draw between $0\mu A$ and $100\mu A$ of current; the value is linearly determined by S_{in}. The JFET is connected to a test input by a shielded coaxial cable which provides noise immunity for rapidly changing test currents. The coax cables for all 36 current-drain input devices have matched impedances.

As stated above, these units latch a new value from the input data bus when they are addressed. They continue to present their previous current-drain signals until they receive the triggering *Xfer.L* signal.

2.2.2 Constant-Voltage Signals

Two signal-DAC functional units are configured to supply constant reference voltages to a circuit under test. Figure 8 shows the units, at addresses **0x44** and **0x45**. Device **0x45** is basically one of the current-drain units without the JFET: it inverts the DAC/op amp output through a second op amp[3] to produce a positive reference voltage, selectable between 0V and 10V based on S_{in}. As originally designed, device **0x44** supplied the negative DAC/op amp output voltage directly to a circuit under test as a negative reference voltage, selectable between 0V and -10V. Presently this output is

also routed through a second op amp, to provide another independent positive reference voltage. In effect both polarities of voltage are available from each unit, requiring only that the appropriate op amp's output be connected to the circuit under test. Coaxial cables identical to the current-drain cables are used. When addressed, these units latch a new value from the input data bus and immediately begin supplying the converted voltage.

2.3 Outputs

Six output functional units are provided, each consisting of the circuit shown in Figure 10 assembled on a prototyping board which is mounted to the aluminum plate. A shared signal causes conversion of up to six test outputs simultaneously; the results may then be retrieved by addressing each unit as desired. The units are addressed from **0xf0** through **0xf5**.

The test circuit's output (assumed to be a current drain of between $0\mu A$ and $100\mu A$) is connected through a shielded coaxial cable, identical to the input cables, to a pair of TL082 op amps which convert the signal to a voltage between 0V and 5V (dependent on the 5V reference circuit shown in Figure 5). This V_{test} voltage is supplied to an ADC1210 ADC chip.

A conversion is initiated by supplying a *Convert.L* pulse, which is gated by the ADC's $\overline{CC}$ output. (It is possible to supply the *Convert.L* pulse to any combination of the six ADCs simultaneously — see §2.4.1). If $\overline{CC}$ is True, the *Convert.L* pulse is latched to the ADC's $\overline{SC}$ input. When the ADC receives $\overline{CC}$, it begins converting the V_{test} to a 12-bit digital value V_{out} by comparing it to the reference provided by the 10V circuit of Figure 5. During the conversion the ADC holds its $\overline{CC}$ signal False. The conversion takes $100\mu sec$ (approximately 12 cycles of the 10V clock from Figure 6), after which the $\overline{CC}$ signal is set True. The 12-bit S_{out} is made available through $47K\Omega$ matching resistors to enabled 74HC245 transceivers.

S_{out} is read from any one of the units when the corresponding address is selected. It enables the appropriate 74HC245 transceivers which copy S_{out} from the ADC onto the output data bus.

An $\overline{SC}$ signal received in the midst of an ongoing conversion would corrupt the conversion; hence the use of $\overline{CC}$ to block *Convert.L* during the conversion time. If a constant *Convert.L* signal were supplied it would generate a train of successive conversions, which is not desirable for the ATB; however, the single-pulser circuitry shown in Figure 12 constrains *Convert.L* to be a single

pulse.

2.4 Timing

The input DACs can be controlled to present their test signals simultaneously even though they have to be loaded individually; the output ADCs can be triggered to convert one or more test outputs at the same time; and must be timed to avoid spurious conversions that would corrupt previously acquired readings.

2.4.1 Triggering inputs and outputs

Figure 11 shows four 74LS273 octal D-flipflops, which serve as control devices at addresses **0x40** through **0x43**. Each of the octal flipflops receives the low-order eight bits of the input data bus, and presents the bits as outputs when the chip is addressed.

When addressed, device **0x40** presents Bit 0 as the *Xfer.L* signal to all of the input DACs; the remaining bits are unconnected.

Device **0x42** presents the low-order six bits as *Sync* signals for each of the six ADCs. The value on the input data bus (1 through 63) determines what combination of ADCs are triggered to perform conversions. The Sync circuit described below converts each of these *Sync* signals to single-clock *Convert.L* pulses, as required by the ADCs.

Devices **0x41** and **0x43** are unused.

2.4.2 Single-pulse generation

Figure 12 shows a single-pulser circuit which is replicated six times. Each copy receives one of the *Sync* signals from device **0x42** and produces a one-clock-cycle *Convert.L* pulse at +10V, which signals the appropriate ADC to begin a conversion. Thus a conversion may be delayed as much as one clock cycle after device **0x42** is addressed (plus signal propagation delays).

2.5 Interface

The interfacing logic between the ATB and the controller is implemented on two "perf" boards mounted at two corners of the platform. They are

connected by a gray ribbon cable which carries address lines A0 through A7 and A18. Data values and device addresses are buffered, sent and received on the Parallel Interface Board. Addresses are decoded and distributed by the Address Decode Board. Input data values are distributed over the input data bus; output data values are collected from the output data bus.

2.5.1 Parallel Interface Board

The Parallel Interface Board communicates with the controller computer and distributes values to and from the functional units of the ATB. It makes use of the "Centronics printer" parallel port design of the early IBM PC desktop computers. This port design supplies eight Data bits which are *not* treated as bidirectional.[4] Four Control bits (three of which are inverted) are also received from the controller, and five Status bits (one inverted) can be returned to the controller. Through these bits, the interface must receive 12-bit data values to be supplied to the ATB units, and return 12-bit values received from the ADCs. It must also receive 8-bit addresses which are used to activate devices on the ATB, plus Control signals that govern operations. In a typical controller architecture the Data bits, Control bits, and Status bits are manipulated and referred to as the "Data Register", the "Control Register", and the "Status Register" respectively (see §3.1). Figure 15 maps these bits to the pins of a DB-25 parallel-port connector plug. Some of the Control and Status bits are inverted by the standard controller hardware; these inversions are compensated for in the controlling software.
Note — "Data" and "Control" in the context of the parallel port are distinct from "input data values" and "controlling signals" as used on the ATB itself. The ATB's "input data values" are transmitted to the ATB through the Data Register of the parallel port; the controlling signals are either from input data bus values or from addresses. The Control Register values described below only control the interfacing logic on the Parallel Interface Board.

[4] Many recent implementations of the PC parallel port design support bidirectional data bits, but IBM's original specification short-sightedly hardwired "write-only" functionality into the design.

Controller to ATB (input). Figure 13 is a schematic of the Parallel Interface Board. The eight Data bits are received and amplified by a 74LS244[5] octal line receiver which routes them to three 74LS374 enabled octal flipflops. The 74LS374s serve as buffers for the low-order eight bits of the ATB's input data bus, the high-order four bits of the input data bus, and eight device address bits. (The address bits are placed on the gray ribbon cable as lines A7 through A0.) The 74LS244 is permanently enabled, while a separately received Control value governs when (and whether) one of the 74LS374s actually latches in the Data bits.

Another 74LS244 receives the four Control bits; bit C_3 is routed to the Address Decode Board as line A18 of the gray address cable, while bits $C_2..C_0$ are passed to a 74LS139 enabled decoder. Bits C_2 and C_1 are decoded to form the enable signals for the 74LS374 flipflops, and C_0 enables the 74LS139 decoder. This allows the correct 74LS374-enable signal to be set up without experiencing glitches. Figure 1 lists the effect of the Control bits.

Getting a value from the parallel port. The general protocol for loading an 8-bit value into the ATB is:

1. Place the value on the Data bits of the parallel port (controller writes the value to its Data Register).

2. Select the desired receiving lines by writing a disabling value to the Control Register — for example, if the value is intended as the low-order bits of an ATB input, the appropriate four Control bits are {0101}.

3. Enable the 74LS139, and hence the desired 74LS374 latch, by writing the enabling form of the Control value to the Control Register — *viz.*, {0100}.

4. Disable the 74LS139 again by rewriting the Control value from Step 2 — *viz.*, {0101}.

[5]Some of the chips used, particularly transceivers, are actually members of the 74HC chip family rather than 74LS. Either family is acceptable on the ATB.

5. Deselect all latches by writing {0001} to the Control Register.

After Step 3 is completed, the value will be presented and held on the appropriate receiving lines of the ATB — high- or low-order input data bus, or address bus — until a new value is latched into that 74LS374.

If the loaded value is in fact a device address, then another Control value will be needed to make the Address Decode Board actually decode the address and issue the corresponding device *Write.L* signal. This Control value is bit C_3, which is routed directly to the Address Decode Board over line A18 of the gray address cable. After the desired address has been loaded onto the address cable (using the above protocol), two more steps pulse the *Write.L* signal:

6. Activate the Address Decode Board by writing {1001} to the Control Register.

7. Repeat Step 5.

Typically a device is activated by loading its address to the ATB and then immediately toggling bit C_3. In this case step 6 can be performed immediately after step 4, and the "Deselect all" value {0001} need only be sent once.

ATB to Controller (output). The Parallel Interface Board also sends output data values back to the controller through the parallel port. Since the original, basic form of the parallel port doesn't provide bidirectional Data bits, the output values are transmitted via the Status Register, four bits at a time. The output data bus lines are connected to two 74LS244 transceivers in three groups of four bits (along with four dummy bits). The 4-bit sections of the 74LS244s are individually enabled, and connected in parallel to the Status bits of the parallel port. As indicated in Figure 1, the output 74LS244s are selected and enabled by the same Control values that select the input 74LS374s, so every time a value is written to the ATB a value is also sent back to the controller's Status Register. It is up to the controller to ignore these values unless it wants them.

Sending a value over the Status lines. A complete 12-bit value must be sent four bits at a time. The protocol for returning a 4-bit value to the controller is somewhat simpler than the loading protocol. First the (12-bit) value must be written onto the output data bus by addressing one of the ADC output units. Four-bit portions of the value are then transmitted as follows:

1. Select the desired bits to receive by writing the appropriate Control Value to the Control Register — for example, to get the low-order four bits, write {0011}.

2. Read the Status Register (within the controller) and mask off the meaningless bits.

3. Repeat steps 1 and 2 for the remaining nybbles.

Note — Each output 74LS244 section can be enabled by four distinct Control values, three of which will also do something else. For example, {0011}, {0010}, {1011}, and {1010} will all send bits OD3..OD0; but setting $C_0 = 0$ will also enable the input 74LS139 decoder, and setting $C_3 = 1$ will issue a *Write.L* to some device. Neither of these additional effects is likely to be desirable. Only the values {0011}, {0101}, and {0111} should be used ({0001} is innocuous, but unnecessary).

2.5.2 Address Decode Board

The Address Decode Board, shown in Figure 14, is basically a large, enabled demultiplexer. It receives eight address bits as lines A0 through A7 and one Control bit as line A18, all from the Parallel Interface Board. Three 74LS244 octal transceivers (one unused) distribute the bits to ten 74LS138 demultiplexers that issue the *Write.L* signals, and one 74LS138 that selects the *Write.L* 74LS138s. Some addresses require an enabling Control value in order to generate a *Write.L* signal, while others generate *Write.L* immediately.

The low-order bits A2..A0 are routed to the *Write.L* 74LS138s, which are labeled in Figure 14 with their corresponding device addresses. Bits A5..A3 are decoded by the Select 74LS138, whose outputs enable the *Write.L* 74LS138s for the DACs at addresses **0x00**..**0x23**. The Select 74LS138 is itself

enabled by bit A18, in conjunction with the address bits $\overline{A7}$ and $\overline{A6}$. Thus the DACs at addresses **0x00**..**0x23** will receive a *Write.L* signal only when Control bit C_3 goes high *and* the high-order two address bits are $\{0\,0\}$.

The Trigger latches and reference DACs at addresses **0x40**..**0x45** get *Write.L* from a 74LS138 that is enabled by bits A18, $\overline{A7}$, and A6. These devices thus receive *Write.L* when Control bit C_3 goes high and the high-order address bits are $\{0\,1\}$.

The ADC transceivers' *Write.L* 74LS138 is enabled by A7 and $\overline{A3}$, so that it issues *Write.L* for addresses **0x80** through **0x87** as soon as the address appears, regardless of C_3. In fact, all addresses whose high-order bit is $\{1\}$ are accepted by this 74LS138; the ADC output units could be addressed as any of **0x80**..**0x85**, **0x90**..**0x95**, ..., **0xf0**..**0xf5** interchangeably. The use of addresses **0xf0**..**0xf5** is arbitrary. Another, unused 74LS138 is similarly enabled by A7 and A3 to issue *Write.L* for addresses **0x88** through **0x8f** and higher-numbered aliases.[6]

2.5.3 Address Mapping

An anomaly in wiring the connection between the between the Parallel Interface Board and the Address Decode Board resulted in swapping the address bits pair by pair: A0 and A1, A2 and A3, A4 and A5, A6 and A7. (Likewise, Control bit C_3 ended up on A18 instead of the intended A19.) Rather than rewire this once it was discovered, the anomaly has been corrected by mapping logical addresses to physical addresses in the software. This is described in §3.1.1.

2.6 Test Circuit

An unoccupied area is available in the center of the ATB. Typically the circuit to be tested is a DIP-mounted "chip" which is held on a prototyping board; the ATB's input and output functional units, which surround the area, are connected to the test circuit board through shielded coaxial cables. Ground connections are made directly to the aluminum plate which forms the floor

[6]The Address Decode Board's design supports the use of some additional addresses; however, additional addresses higher than **0x80** will require a redesign of the board, at which time the aliasing should be removed.

of the unoccupied area. Figure 3 depicts two separate test circuits, "KLLA" and "null", positioned within the area.

Figure 4 details a typical test circuit and its electrical connections to the ATB. The Cmir_1 analog current-mode circuit is part of the author's KLLA test chip ([MM93]). The circuit receives inputs from pins 11 and 12 and delivers its output to pin 9 of the KLLA chip. It also uses the chip-wide reference voltage and ground (supplied to pins 30 and 10), and the chip's pads all require a comparable voltage and ground (supplied to pins 5 and 35) for proper operation. This circuit will compute the Łukasiewicz implication function, a ramp-like function. An example of this circuit's output is plotted in Figure 17.

2.7 Digital Test Circuits

A digital circuit can be easily tested on the ATB, if no more than 12 bits of input are required; six sets of 12 simultaneously captured output bits can also be collected. The procedure is to simply jumper from the input data bus to the test circuit's inputs, bypassing the DAC units entirely. (However, the point of connection of a DAC unit to the input data bus is a convenient place to put the jumpers.) The DAC *Write.L* and *Xfer.L* signals are unnecessary. A lower-level interface control is needed to put the desired input bits onto the input data bus.

Alternatively, all of the DAC units can be used in the same way as devices **0x44** and **0x45**, by tapping the voltage outputs of the op amps as single-bit inputs. This approach provides 38 bits of input which must be set up individually; however, positive- and negative-voltage inputs are available, and intermediate voltage levels are available for exploring low-voltage devices and non-saturated behaviors.

Output data bits can be similarly jumpered to the inputs of an ADC unit's 74HC245 transceivers, and the appropriate ADC addressed to read the output bits back to the controller. The ADC *Convert.L* signal is not required, since the ADC chip isn't involved. Up to 12 bits can be read simultaneously, and up to six different sets of 12 can be captured.

3 ATB Control

The ATB exercises a test circuit by providing input signals and recording output signals under the control of a computer equipped with a "Centronics" style parallel port. This section describes the control algorithms and software as implemented on an MS-DOS desktop computer based on an 80386 CPU with an 80387 floating-point coprocessor.[7] The machine in use has a parallel port with Data, Status, and Control Registers at I/O addresses 0x0378, 0x379, and 0x37a ($0378, $0379, $037A in Intel notation). Values are sent to the ATB by writing the Data and Control Registers, and received from the ATB by reading the Status Register. The software described here is written in Turbo C version 2.0, an ANSI-standard implementation of the C language with extensions suited to the Intel 8086 architecture. In particular, Turbo C offers two port-I/O functions:[8]

`void outportb(char Byte, char Address)`
— writes an 8-bit byte to an I/O register

`char inportb(char Address)`
— returns an 8-bit value from an I/O register

The controlling algorithms are described in bottom-up order, from the lowest-level hardware control operations up to overall testing procedures. Algorithms are expressed as functions in ANSI-C notation. Appendix A.1 lists the actual library subroutines used by the author to control the ATB, and Appendix A.2 shows a testing program that uses the library.[9]

3.1 Interface Operations

The fundamental operations that the controlling computer can perform are to place values on the ATB's input data bus, generate device-enabling *Write.L*

[7] The math coprocessor is not required, but speeds up some of the data manipulation substantially.

[8] Other languages may include comparable instructions. The underlying assembly-language instructions are `OUT` and `IN`.

[9] The original code has been debugged with much effort and is known to work; but with hindsight it seems rather like "a twisty maze of little passages, all different". The examples used in the text should be rather clearer, and might be preferable in actual use.

signals, and read values from the ATB's output data bus. These operations involve the Parallel Interface Board's buffering hardware, which is operated by the computer via the Control Register bits. Typically the Data Register is located at I/O Port address 0x0378; other common addresses are 0x0278 and 0x03bc. The Status Register's address is [Data register]+1; the Control Register's address is [Data Register]+2. As indicated in §2.5.1 and Figure 15, three of the Control Register bits are inverted relative to the electrical signals sent out. An "exclusive-OR" mask in the code below does the bitwise inversion of program values that are written to the Control Register.

3.1.1 Sending Data

Two kinds of data are sent to the ATB: 12-bit values for the input data bus, and 8-bit addresses. 12-bit values are transmitted as an 8-bit lower chunk and a 4-bit upper chunk, sent in either order.s[10] A data-value chunk is sent by placing it on the Data lines of the parallel port and instructing a latch on the Parallel Interface Board to accept the chunk, using the Control Register values listed in Figure 1. A complete 12-bit value takes two steps. A C function that puts a 12-bit value on the input data bus is:

```
/* I/O Register addresses: */
#define D_Reg        0x0378    /* Data-Register       */
#define C_Reg        0x037a    /* Control-Register    */
#define CTRL_X_MASK  0x0b      /* fixes inverted bits */
#define CTRL_null    0x01      /* Nothing enabled     */

void send_12bits(unsigned char Upper, unsigned char Lower)
{
    /* ID11..ID8 onto data bus */
    outportb(D_Reg, Upper);
    /* Select high-chunk latch */
    outportb(C_Reg, 0x03 ^ CTRL_X_MASK);
    /* Select latch, enable '139 */
    outportb(C_Reg, 0x02 ^ CTRL_X_MASK);
```

[10] Partial values can also be sent, changing only some of the bits on the input data bus. Doing this would require care to keep track of what value is actually present, since there is no way to read the input data bus.

```
    /* Drop enable bit again */
    outportb(C_Reg, 0x03 ^ CTRL_X_MASK);

    /* ID07..ID0 onto data bus */
    outportb(D_Reg, Lower);
    /* Select low-chunk latch */
    outportb(C_Reg, 0x05 ^ CTRL_X_MASK);
    /* Select latch, enable '139 */
    outportb(C_Reg, 0x04 ^ CTRL_X_MASK);
    /* Drop enable bit again */
    outportb(C_Reg, 0x05 ^ CTRL_X_MASK);

    /* Turn everything off */
    outportb(C_Reg, CTRL_null ^ CTRL_X_MASK);
}
```

An address is sent similarly, substituting `0x07` and `0x06` (the Address-latch "address") for `0x03`/`0x02` or `0x05`/`0x04`. The ATB device addresses **0x00..0x23** and **0x40..0x45** also require an address-enable command via bit 3 of the Control Register. As mentioned in §2.5.1, this can be sent immediately after the address is latched in, like so:

```
void send_DAC_address(unsigned char Addr)
{
    /* A7..A0 onto data bus */
    outportb(D_Reg, Addr);
    /* Select address latch */
    outportb(C_Reg, 0x07 ^ CTRL_X_MASK);
    /* Select latch, enable '139 */
    outportb(C_Reg, 0x06 ^ CTRL_X_MASK);
    /* Drop enable bit again */
    outportb(C_Reg, 0x07 ^ CTRL_X_MASK);

    /* enable DAC addresses with 0000_1001, i.e. bit C_3  */
    outportb(C_Reg, 0x09 ^ CTRL_X_MASK);

    /* Turn everything off */
    outportb(C_Reg, CTRL_null ^ CTRL_X_MASK);
```

```
}
```

The code in Appendix A.1 is slightly more layered — it provides a lowest-level `latch_in()` function that latches a byte to the Parallel Interface Board, and `set_data()` and `set_addr()` functions that make use of it to send 12-bit input data values and 8-bit addresses.

Generating addresses. As mentioned in §2.5.3 the logical device addresses must be mapped to the physical addresses that the ATB interface logic sees, to compensate for a wiring error: address bits get swapped in a pairwise fashion. A function that fixes this is:

```
unsigned char physical_address(unsigned char Logical_Address)
{
    int i;
    unsigned char Physical_Address, b1, b0;
    Physical_Address = 0;
    for (i = 0; i <= 7; ++i) {
        /*
        | Pick off the 2 highest-order bits, and shift the
        | address left in preparation for the next loop.
        */
        b0 = 0x80 & Logical_Address;
        b1 = 0x40 & Logical_Address;
        Logical_Address <<= 2;

        /*
        | Shift the bits down to low order, swapping them in
        | the process, and "OR" them onto the mapped address.
        */
        Physical_Address = (Physical_Address << 2)
                         |  (b0 >> 7)  |  (b1 >> 5);
    }
    return Physical_Address;
}
```

However, the library code in Appendix A.1 uses a faster and simpler solution — a logical-to-physical-address lookup table implemented as the array

`Addr_Map[256]`.[11] This is invoked in the low-level function `set_addr()`, so the address mapping is invisible to user-level testing programs and even to the rest of the library routines.

3.1.2 Retrieving Values

The output data bus of the ATB provides 12-bit values, which must be read through the Status Register in 4-bit nybbles. (A fourth nybble is available, and provides zeros for bits OD15..OD12.) The nybbles may be read in any order, and must be shifted and concatenated to form a complete (16-bit) value. As with the Control Register, one of the Status Register bits is inverted in the hardware, so an "exclusive-OR" mask is used to adjust this. The following function reads the ATB and returns a 12-bit value as a 16-bit integer:

```
#define S_Reg          0x0379  /* Status-Reg. I/O address */
#define STATUS_X_MASK  0x80    /* fixes inverted bit 7 */

unsigned int receive_12bits(void)
{
    unsigned int Twelve, Four;

    /*
    | Latch bits OD3..OD0 from the output data
    | bus into the Status Register, read them,
    | & copy them into the variable 'Twelve'
    */
    outportb(C_Reg, (0x03 ^ CTRL_X_MASK));
    Four = inportb(S_Reg) ^ STATUS_X_MASK;
    Twelve = (Four & 0x00f0) >> 4;

    /*
    | Latch and read bits OD7..OD4,
    | & copy them into 'Twelve'
    */
```

[11] Depending on the programming language used, this can also be a shorter solution.

```
    outportb(C_Reg, (0x05 ^ CTRL_X_MASK));
    Four = inportb(S_Reg) ^ STATUS_X_MASK;
    Twelve = Twelve | (Four & 0x00f0);

    /*
    | Latch and read bits OD11..OD8,
    | & copy them into 'Twelve'
    */
    outportb(C_Reg, (0x07 ^ CTRL_X_MASK));
    Four = inportb(S_Reg) ^ STATUS_X_MASK;
    Twelve = Twelve | (Four & 0x00f0) << 4;

    return Twelve;
}
```

This function appears (in somewhat baroque form) as `ADC_bus()` in Appendix A.1.

3.2 ATB Device Operations

The basic operations that the ATB performs are:

- Load a value into a DAC input device.
- Convert input values to test-input current drains.
- Trigger test-output conversions.
- Read ADC output values.
- Initialize the ATB.

These actions are commanded by sending the appropriate data and addresses to the ATB using the algorithms defined in §3.1.

3.2.1 Load a Value into a DAC

This operation is straightforward: put the desired value onto the input data bus, then address the desired DAC to take the value. Values must be in the 12-bit range from `0x00..0xfff` (0..4095), and the valid DAC addresses are

0x00..**0x23** and **0x40**, **0x42**..**0x45**. (Two of these, **0x40** and **0x42**, aren't actually DACs, but they operate in the same way.)

```
void load_DAC(unsigned char DAC_addr, unsigned int Value)
{
    unsigned char Upper, Lower;
    Lower = (unsigned char)(Value & 0x00ff);
    Upper = (unsigned char)((Value & 0xff00) >> 8);
    send_12bits(Upper, Lower);
    send_DAC_address(DAC_addr);
}
```

3.2.2 Convert Test-Input Values

The test-current DACs at addresses **0x00**..**0x23** can operate in "double-buffered" or "flow-through" mode. In the normal double-buffer mode the DACs simultaneously convert the values they've been loaded with, only when they receive the shared *Xfer.L* signal from device **0x40**. Once they start converting, *Xfer.L* can be turned back off and they will maintain the conversion; meanwhile, a new value can be loaded in preparation for another *Xfer.L* conversion signal. Device **0x40** issues *Xfer.L* when it is loaded with the value `0x01`, and turns off *Xfer.L* when loaded with `0x00`:

```
void Xfer_on(void)
{
    load_DAC(0x40, 0x01);
}

void Xfer_off(void)
{
    load_DAC(0x40, 0x00);
}
```

In the alternative flow-through conversion mode, each DAC begins converting a new value as soon as the value is loaded, independently of the other DACs. Flow-through mode can be turned on by calling `Xfer_on()` initially and leaving it that way; flow-through mode will be turned off again whenever `Xfer_off()` is called.

3.2.3 Trigger Test-Output Conversions

The ADC output units convert the test-output currents they see to 12-bit values, when they get a *Convert.L* signal. Each ADC receives its own *Convert.L* from device **0x42**, which generates the signals from the low-order six bits of the ATB input data bus. Writing **0x42** with `0x011`, for example, generates *Convert.L* for ADC 5 (at address **0xf5**) and ADC 0 (at address **0xf0**). The *Convert.L* signals are triggered by a transition from "bit-Off" to "bit-On", so the appropriate bit in device **0x42** must start at 0 and change to 1. The following function assures this by forcing all bits to 0 initially. For each ADC to be triggered, the corresponding function argument should be set to 1. Untriggered ADCs should have their arguments set to 0.

```
void trigger_ADC(int adc0, int adc1, int adc2,
 int adc3, int adc4, int adc5)
{
    unsigned char adcs;

    /*
    | OR together all the desired ADC arguments:
    */
    adcs = ( ((adc5 != 0) << 5)
            |  ((adc4 != 0) << 4)
            |    ((adc3 != 0) << 3)
            |      ((adc2 != 0) << 2)
            |        ((adc1 != 0) << 1)
            |           (adc0 != 0)
           );

    /*
    | Turn off all Convert.L signals first, then
    | Trigger the desired ones:
    */
    load_DAC(0x42, 0x00);
    load_DAC(0x42, adcs);
}
```

The library function `ADC_sample()` in Appendix A.1 just accepts the 8-bit `adcs` value, and leaves it to the calling function to perform the multiple `OR` if more than one ADC is to be triggered simultaneously. This avoids the overhead for single-ADC operation.

3.2.4 Read ADC Output Values

Reading an ADC's converted output is a two-step operation: first command it to put its value on the ATB output data bus by addressing it, then read the output data bus through the Status Register. Unlike the DAC addresses, the ADC output unit addresses **0xf0**..0xf5 do not require the C_3 enable signal; on the other hand, the ADC's output is present on the output data bus only as long as it is being addressed, so addressing and ADC and reading its value must be a more-or-less atomic operation.

```
unsigned int read_ADC(unsigned char Addr)
{
    unsigned int ADC_val;
    /*
    | Send the ADC's address like other addresses,
    | but without the unneeded enabling Control bit:
    */
    outportb(D_Reg, Addr);
    outportb(C_Reg, 0x07 ^ CTRL_X_MASK);
    outportb(C_Reg, 0x06 ^ CTRL_X_MASK);
    outportb(C_Reg, 0x07 ^ CTRL_X_MASK);
    outportb(C_Reg, CTRL_null ^ CTRL_X_MASK);

    ADC_val = receive_12bits();

    /*
    | Disable the ADC output again.  (Not really necessary.)
    */
    outportb(D_Reg, 0x3f);
    outportb(C_Reg, 0x07 ^ CTRL_X_MASK);
    outportb(C_Reg, 0x06 ^ CTRL_X_MASK);
    outportb(C_Reg, 0x07 ^ CTRL_X_MASK);
    outportb(C_Reg, CTRL_null ^ CTRL_X_MASK);
```

```
    return ADC_val;
}
```

There is no exactly comparable library function. Instead `ADC_sample()` combines the ADC-triggering and -reading steps; the action of disabling the ADC output by erasing its address occurs implicitly when the ADC triggers are reset (by writing `0x00` to device **0x42**) at the end.

3.2.5 Initialize the ATB

This operation just brings the ATB back to a known, inactive state by writing null control values to the ATB devices and the Parallel Interface Board.

```
void reset_ATB(void)
{
    /* Disable all interface latches and DAC addresses. */
    outportb(C_Reg, 0x01 ^ CTRL_X_MASK);

    /* Turn off DAC conversions. */
    Xfer_off();

    /* Ready ADCs for new conversions. */
    load_DAC(0x42, 0x00);

    /* Disable interface latches and DAC addresses again. */
    outportb(C_Reg, 0x01 ^ CTRL_X_MASK);
}
```

3.3 Test Inputs and Outputs

3.3.1 Input Currents and Voltages

The ATB provides two kinds of test input: current drains in the range $0\mu A$ to $100\mu A$ from devices **0x00** through **0x23**, and voltages in the ranges $0V$ to $+10V$ and $0V$ to $-10V$ from devices **0x44** and **0x45**. All devices are set by a 12-bit data value, so the current drains and voltages are available in linear steps of 1/4095 from minimum to maximum. A testing program needs to do something like the following for the test-current DACs:

```
#define Max_Current 100.0

void set_current(unsigned char Addr, float Idrain)
{
    unsigned int Int_Current;
    if ( (Idrain < 0.0) || (Max_Current < Idrain) ) {
        /* Cope with Current-Out-of-Range Error */
    }
    if ( Addr > 0x23 ) {
        /* Cope with Invalid_DAC Error */
    }

    /*
    | Convert user units to an ATB value and send the value:
    */
    Int_Current = (unsigned int)
                  ( (float)0xfff * Idrain/Max_Current );
    load_DAC(DACnum, Int_Current);
}
```

After this is done for all desired DACs, the new values should be converted with an *Xfer.L* pulse:

```
void convert_new_values(void)
{
    Xfer_on();
    Xfer_off();
}
```

The test-voltage DACs at addresses **0x44** and **0x45** are hardwired for flow-through operation, so the *Xfer.L* pulse is unneeded. This function sends out a new reference voltage immediately:

```
#define Max_Volts 10.0
void set_volts(unsigned char Addr, float Volts)
{
    unsigned int Int_Volts;
    if ( (Volts < 0.0) || (Max_Volts < Volts) ) {
```

```
        /* Cope with Voltage-Out-of-Range Error */
    }
    if ( (Addr != 0x44) && (Addr != 0x45) ) {
        /* Cope with Invalid-DAC Error */
    }

    /*
    | Convert user units to an ATB value and send the value:
    */
    Int_Volts = (unsigned int)
                ( (float)0xfff * Volts/Max_Volts );
    load_DAC(Addr, Int_Volts);
}
```

Whether the resultant test voltage is positive or negative is determined by the way the voltage-input unit is connected to the test circuit (see §2.2.2 and Figure 8).

3.3.2 Test Output Readings

The `read_ADC()` function described above returns test outputs as 12-bit values representing a fraction of the range $0\mu A$ to $100\mu A$. A single ADC can be triggered and read as follows:

```
float sample_test_current(ADC_addr)
{
    unsigned char adc;
    float fraction;
    if ( (ADC_addr < 0xf0) || (0xf5 < ADC_addr) ) {
        /* Cope with Invalid-ADC Error */
    }

    /*
    | Determine the ADC-trigger bit, turn off all
    | the Convert.L signals, and trigger the
    | desired ADC to convert:
    */
    adc = 1 << (0x07 & ADC_addr);
```

```
    load_DAC(0x42, 0x00);
    load_DAC(0x42, adc);

    /*
    | Read the ADC output and put it in user units:
    */
    fraction = (float)read_ADC(ADC_addr) / (float)0xfff;
    return ( Max_Current * fraction );
}
```

For repeatability and precision studies the 12-bit values may be more important than the equivalent currents; so the library current-input and output routines use 12-bit values exclusively. If engineering units are important the calling program must do its own conversions. Test-input voltage routines are available that work in voltage units for convenience.

3.4 Testing and Data Collection

3.4.1 General Testing

The C-language program `ftntest`, listed in Appendix A.2, is a general-purpose testing program which uses the `atbpara` library. This program presents a menu of low- and middle-level commands for the ATB; the menu screen is shown in Figure 16. `ftntest` was originally written as a board-debugging tool, but creeping featurism has evolved it into a program that can exercise and collect data from test circuits as well.

`ftntest` uses the following functions or macros from the `atbpara` library:

`adc_bus()`

`adc_sample()`

`adc_strobe()`

`adjust_Vdd()`

`adjust_Vss()`

`set_addr()`

`set_data()`

`write_device()`

It also uses some functions that are unrelated to the ATB (and reflect idiosyncrasies of the author). Appendix A.3 shows these additional functions. To round things out, a "makefile" for the `ftntest.exe` program and `atbpara.lib` library is given in Appendix A.4. This makefile uses features of the Borland "make v3.5" program, which is slightly more flexible than the "make" which accompanies Turbo C v2.0.

3.4.2 A Sample Test of KLLA

A simple test of the KLLA analog chip illustrates the use of `ftntest`. The chip's I/O pads are powered by device **0x45**; the Cmir_1 subcircuit only requires two inputs, which have been connected to devices **0x08** and **0x09a**. As shown in Figure 16, the program's output is captured to an output file by the '>' function (which prompts for a file name, here "demo.out"). Subsequent actions are recorded in the file, and data collections are written out, in a format compatible with the `gnuplot` plotting program. The output file is shown in Figure 18, and records the following actions.

The 'V' function sets device **0x45** to 10V to provide I/O power (the -Vss value is unimportant for this test). The 'w' functon is used to set the DAC-**0x08** input to three current levels (high, low, medium); at each level the 'l' function is used to sweep the DAC-**0x09** input over a range of values and record the output from ADC **0x04**.

Figure 17 shows the three output curves, plotted by supplying the output file to `gnuplot`.

4 Acknowledgements

Charles Daffinger conceived, designed, and built the Analog Test Board for his testing purposes. William Hunt traced the wiring and circuits shown in the circuit diagrams, and instructed the author in the parallel interface design. Professor J.W. Mills provided encouragement and motivation to us all, not to mention funding for the materials and time that went into the board. William Hunt and "TJ" Jones were very helpful in obtaining first an 8088-based IBM PC and later an 80386-based personal computer to operate it.

References

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[Mil91] Jonathan W. Mills. Area-efficient implication circuits for very dense łukasiewicz logic arrays. Technical Report 339, Indiana University, Bloomington, IN, November 1991.

[MM93] R. A. Montante and J. W. Mills. Probabilistic error correction in arbitrarily large łukasiewicz logic arrays. Technical Report 377, Indiana University, Bloomington, IN, April 1993.

[PW87] Franklin . Prosser and David Winkel. *the Art of Digital Design.* P T R Prentice Hall, Englewood Cliffs, New Jersey, 2nd edition, 1987.

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Control bits				Input Meaning:		Output Meaning:
C_3	C_2	C_1	C_0	Latch Select	Latch Enable?	Transceiver Select
x	0	0	1	none	Disable	(OD15..OD12)
x	0	1	1	ID11..ID8	Disable	OD3..OD0
x	1	0	1	ID7..ID0	Disable	OD7..OD4
x	1	1	1	A7..A0	Disable	OD11..OD8
x	0	0	0	none	(Enable)	(OD15..OD12)
x	0	1	0	ID11..ID8	Enable	OD3..OD0
x	1	0	0	ID7..ID0	Enable	OD7..OD4
x	1	1	0	A7..A0	Enable	OD11..OD8
0	x	x	x	Disable *Write.L*		-
1	x	x	x	Enable *Write.L*		-

Figure 1: Meanings of Control bits

'x' means "don't care". The C_3 bit has no effect on the latches or transceivers, but should be held at '0' when sending or receiving Data values to avoid writing to a device inadvertently. Bits $C_2..C_0$ similarly have no effect on the *Write.L* signals. OD15..OD12 are hardwired to 0.

Block label in Figure 3:	Detailed in...
KLLA, null	Figure 4
0x00, **0x01**, ..., **0x23**	Figure 9
0xf0 .. **0xf5**	Figure 10
0x40 .. **0x43**	Figure 11
0x44, **0x45**	Figure 8
Vref0, Vref1	Figure 7
ADCref	Figure 5
Clock	Figure 6
Sync	Figure 12
Parallel Interface	Figure 13
Address Decode	Figure 14
Power, ID11..ID0, OD11..OD0	none

Figure 2: ATB schematic/Circuit Diagram Cross References

The ATB schematic in Figure 3 shows functional units which are detailed in the other figures as listed here.

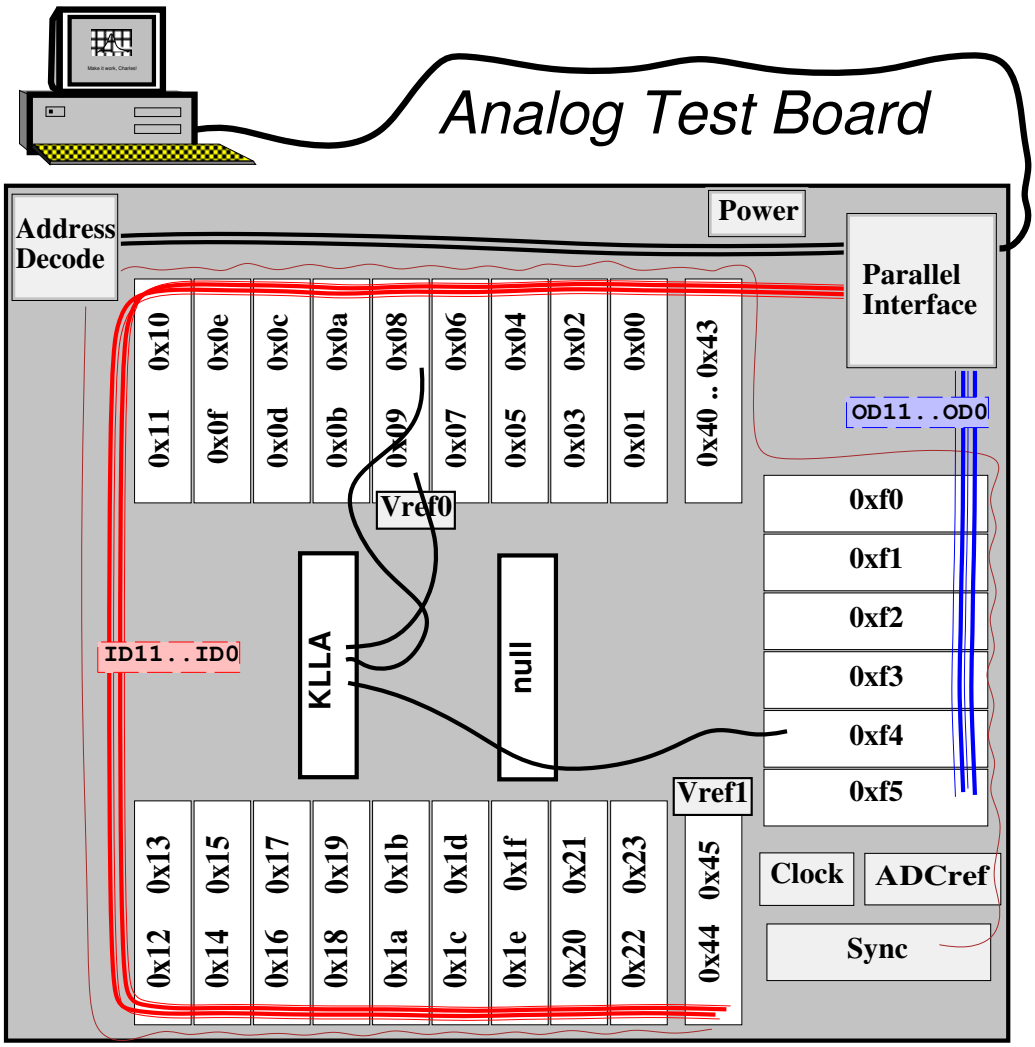

Figure 3: Analog Test Board Schematic
Major functional units on the ATB. Controllable devices are labeled with their addresses in hexadecimal. "Power" identifies the external power-supply connector. "KLLA" and "null" represent typical test circuits, with some connections to KLLA shown. Functional blocks are detailed in following figures; see Figure 2 for cross-references.

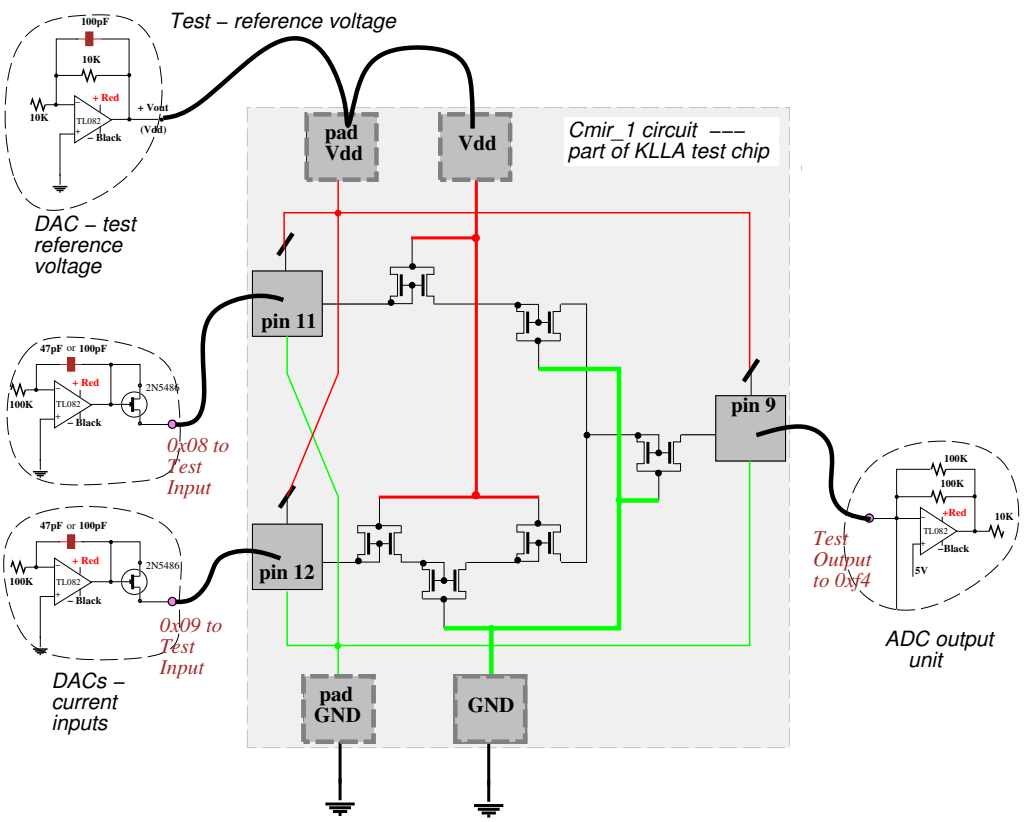

Figure 4: Connecting an analog circuit to the ATB
Portions of the test-reference-voltage circuit (Figure 8), test-current circuits (Figure 9), and test-output circuit (Figure 10) are shown connected to a typical current-mode test circuit. The circuit is typically a DIP chip mounted on a prototyping board; the connections are made through shielded coaxial cables to pins on the chip.

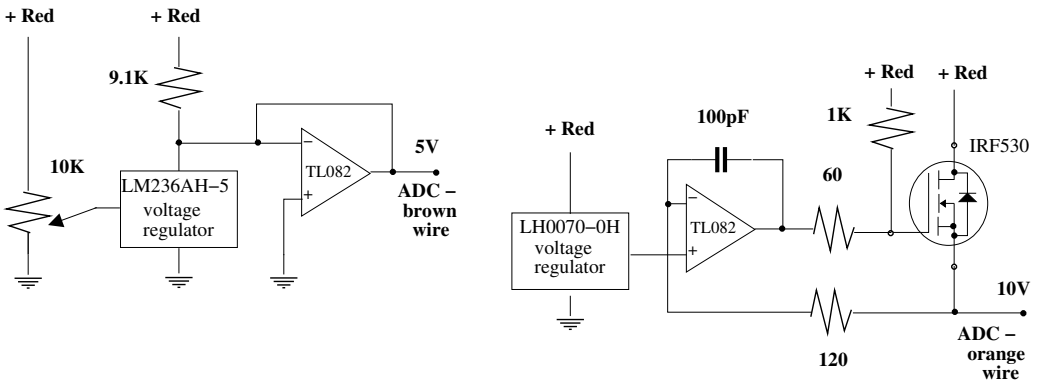

Figure 5: ADC reference voltages
These two circuits provide stable reference voltages for the Analog-Digital Conversion circuits. The voltages are routed through brown and orange wires. "+Red" is the external +15V supply.

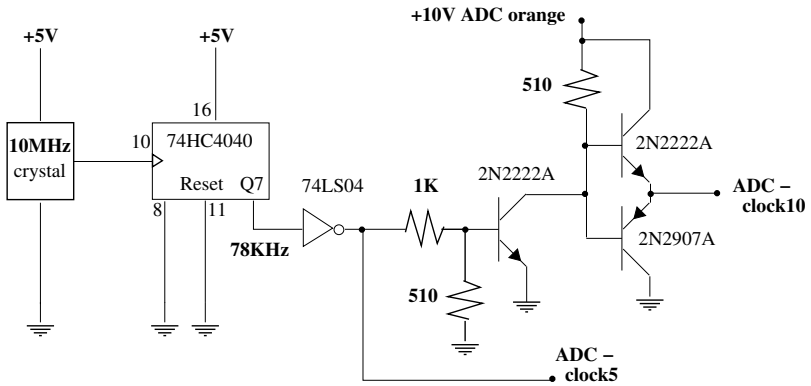

Figure 6: ADC Clock circuit
This crystal-controlled clock circuit provides a 78KHz clock at 5V for the output transceiver chips, and at 10V for the ADC chips.

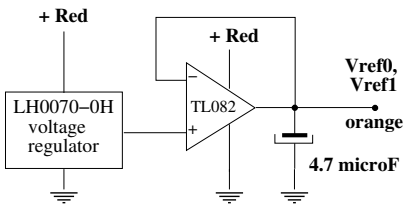

Figure 7: DAC reference voltages
Two copies of this circuit, $V\text{ref}_0$ and $V\text{ref}_1$, provide 10V references to the DAC circuits in Figures 8 and 9.

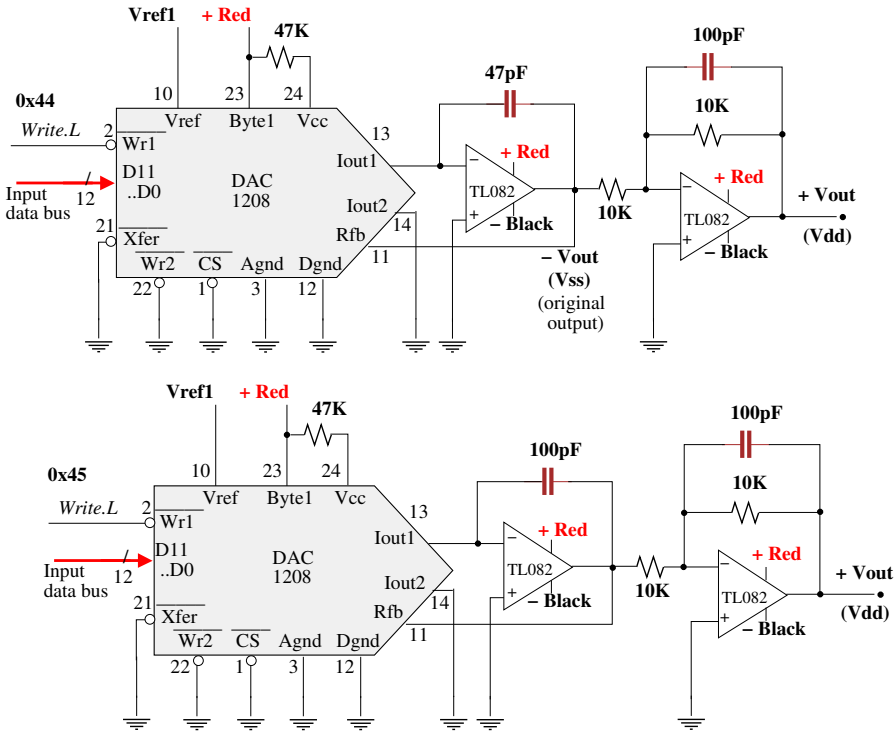

Figure 8: Test-circuit Reference Voltages
These two circuits supply a selectable reference voltage to the test circuit. Either device can supply a negative voltage (Vss) from the output of the leftmost op amp, or a positive voltage (Vdd) from the output of the rightmost op amp.

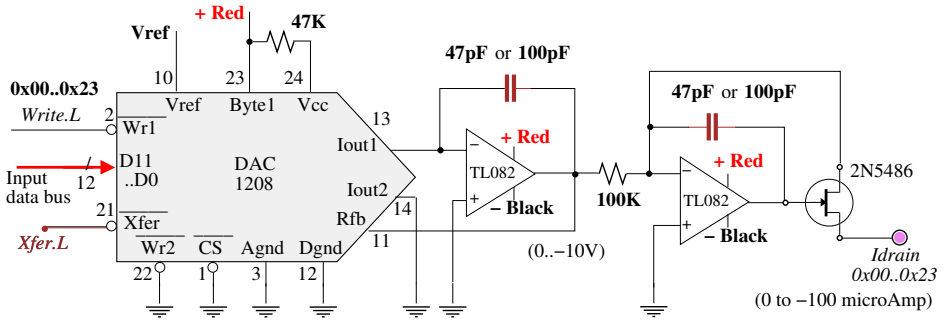

Figure 9: Test-circuit Inputs

Thirty-six copies of this circuit, with addresses from **0x00** to **0x23**, supply selectable currents to test inputs. The currents are *drains*, i.e. positive charge flows *from* the test inputs *to* the 2N5486 transistor.

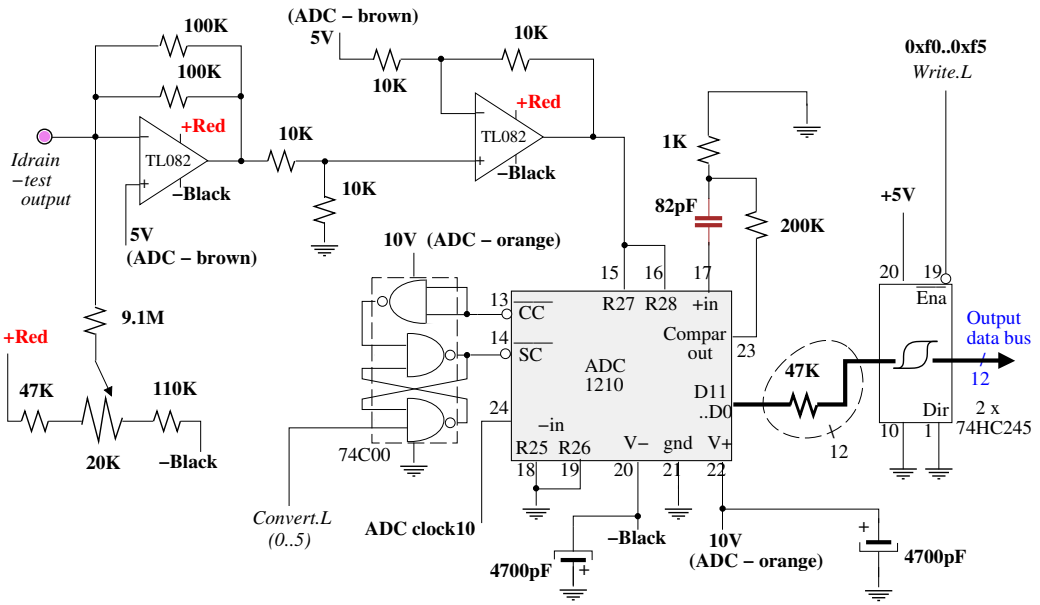

Figure 10: Test-circuit Outputs

Six copies of this circuit, addressed from **0xf0** to **0xf5**, digitize test outputs and supply 12-bit values to the output data bus. Test outputs are assumed to be current *drains*, i.e. positive charge flows *from* the leftmost op amp *to* the test circuit.

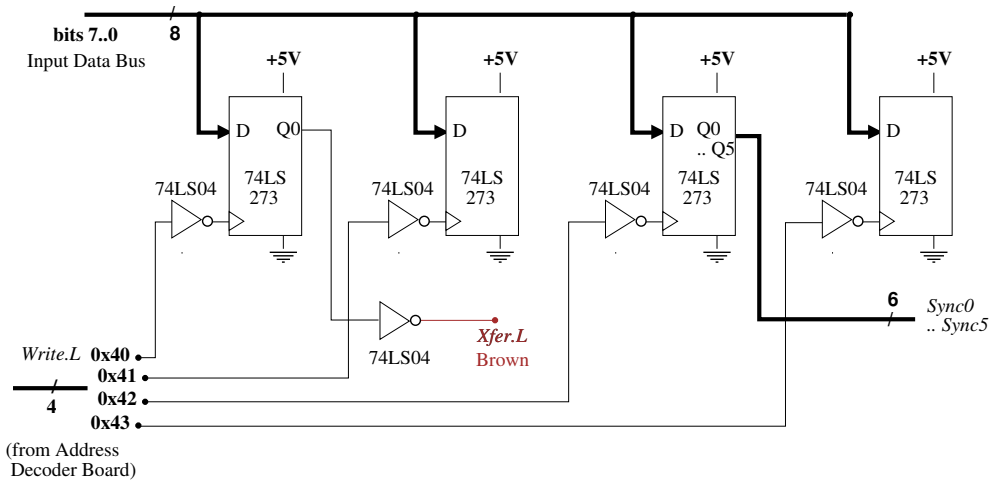

Figure 11: Triggering devices

These "devices" generate triggering signals for the DACs and ADCs when addressed. Device **0x40** uses bit 0 of the input data bus to determine whether the DACs actually receive an *Xfer.L* signal. Device **0x42** uses bits 0..5 to determine which ADCs get a *Sync* (and hence *Convert.L*) signal. (Devices **0x41** and **0x43** are unused.)

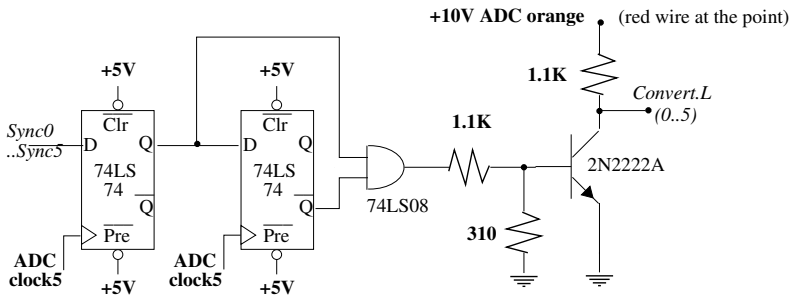

Figure 12: Conversion Synchronization

Six copies of this circuit convert each of the ADC *Sync* signals, from device **0x42**, to single-clock-cycle *Convert.L* pulses that trigger the appropriate ADC to begin a conversion.

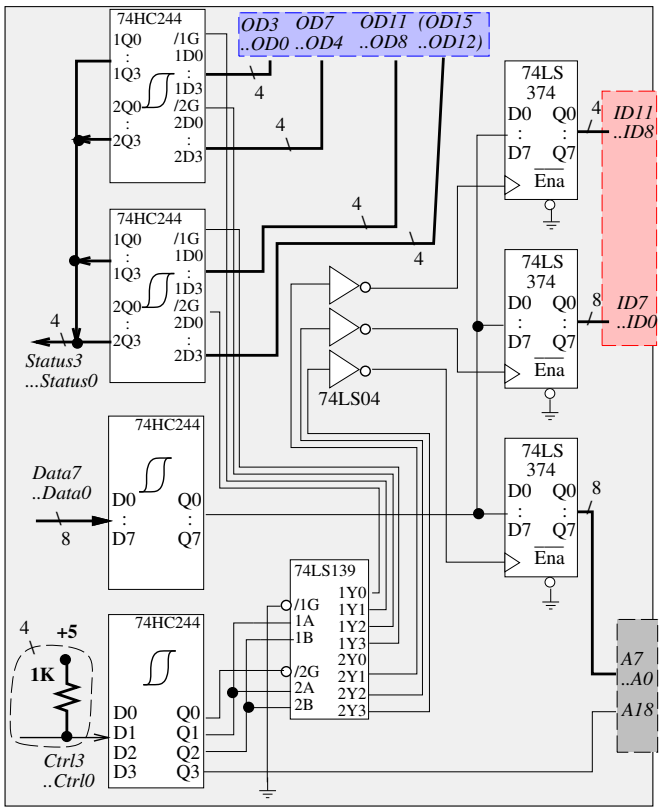

Figure 13: Parallel Interface Board

This circuit board buffers and distributes values to and from the various functional units on the ATB, in conjunction with the Address Decode Board.

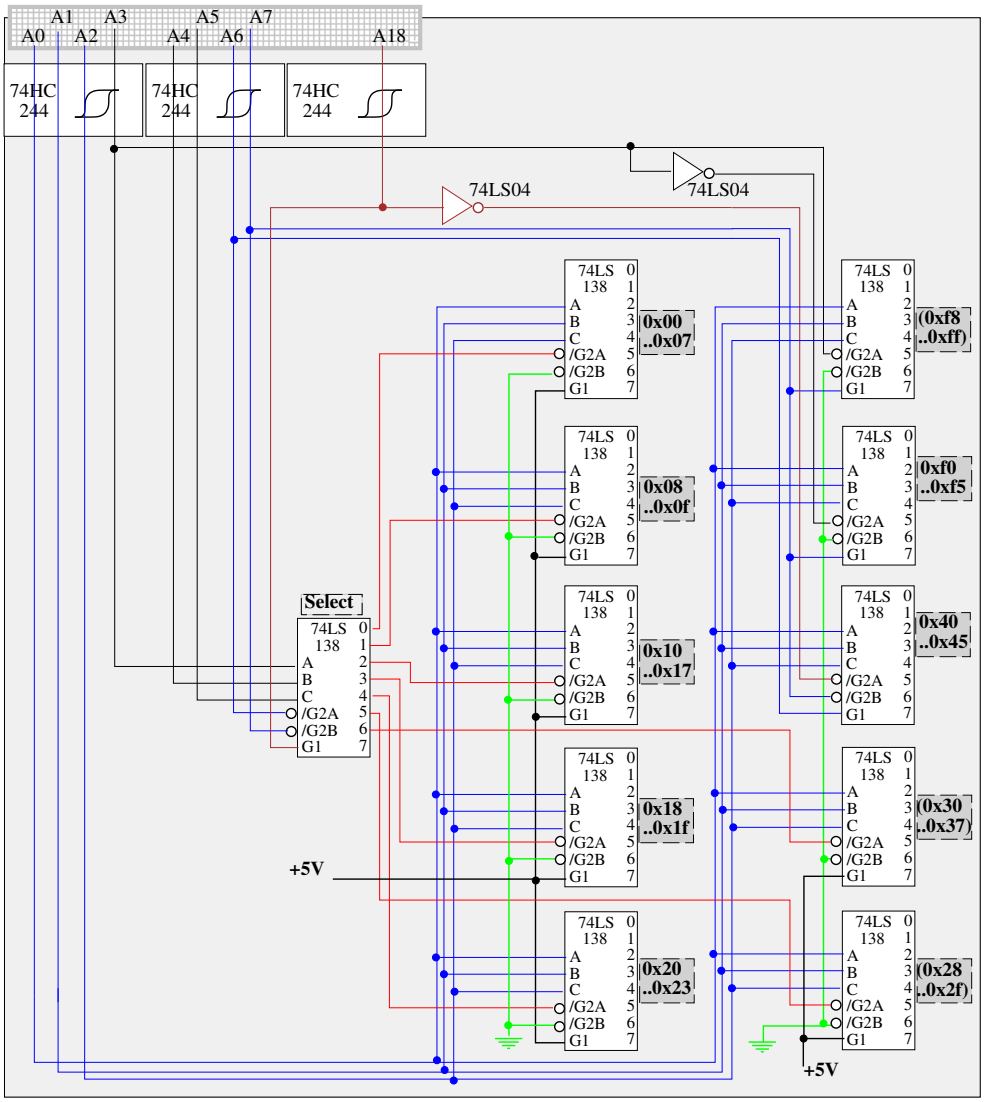

Figure 14: Address Decode Board

This circuit board decodes address lines A7..A0 to activate devices on the ATB. The 74LS138 chips issue *Write.L* signals for the device addresses they are labeled with.

Interface Signal	I/O Register Bit	DB-25 Connector Pin		I/O Register Bit	Interface Signal
$/C_0$	!Ctrl 0	1	14	!Ctrl 1	$/C_1$
D_0	Data 0	2	15	Status 3	-
D_1	Data 1	3	16	Ctrl 2	C_2
D_2	Data 2	4	17	!Ctrl 3	$/C_3$
D_3	Data 3	5	18	-	(Ground)
D_4	Data 4	6	19	-	(Ground)
D_5	Data 5	7	20	-	(Ground)
D_6	Data 6	8	21	-	(Ground)
D_7	Data 7	9	22	-	(Ground)
S_2	Status 6	10	23	-	(Ground)
$/S_3$	!Status 7	11	24	-	(Ground)
S_1	Status 5	12	25	-	(Ground)
S_0	Status 4	13			

Figure 15: Parallel-port pinouts

I/O Register bits are electrically connected to pins of a DB-25 female connector, with corresponding ATB interface signals. Register bits/connector pins are mapped to the ATB Parallel Interface signals as shown.

'-' No connection.

'!' Register bit is inverted relative to its corresponding pin (*e.g.*, [Ctrl bit 1 = 0] implies [pin 14 = 5V]).

'/' Signal is negated (due to the register/pin inversion).

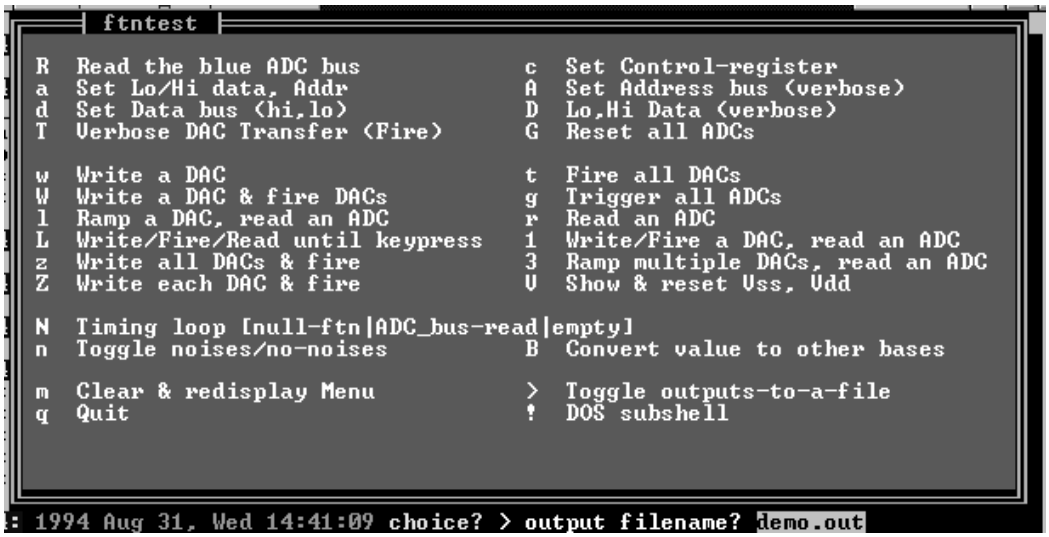

Figure 16: `ftntest` Command Menu

The `ftntest` screen shows available commands. Commands with output overwrite the menu, which can be redrawn when needed. Output can also be copied to a file: here the user has entered the '>' command, which prompts for a filename, and the user has given "demo.out".

The output file is shown in Figure 18, after the command sequence

{'V', 'w', 'l', 'w', 'l', 'w', 'l', 'q'}

is used to exercise the Cmir_1 circuit. The 'V', 'w', and 'l' commands prompt for values.

Figure 17 graphs the output file.

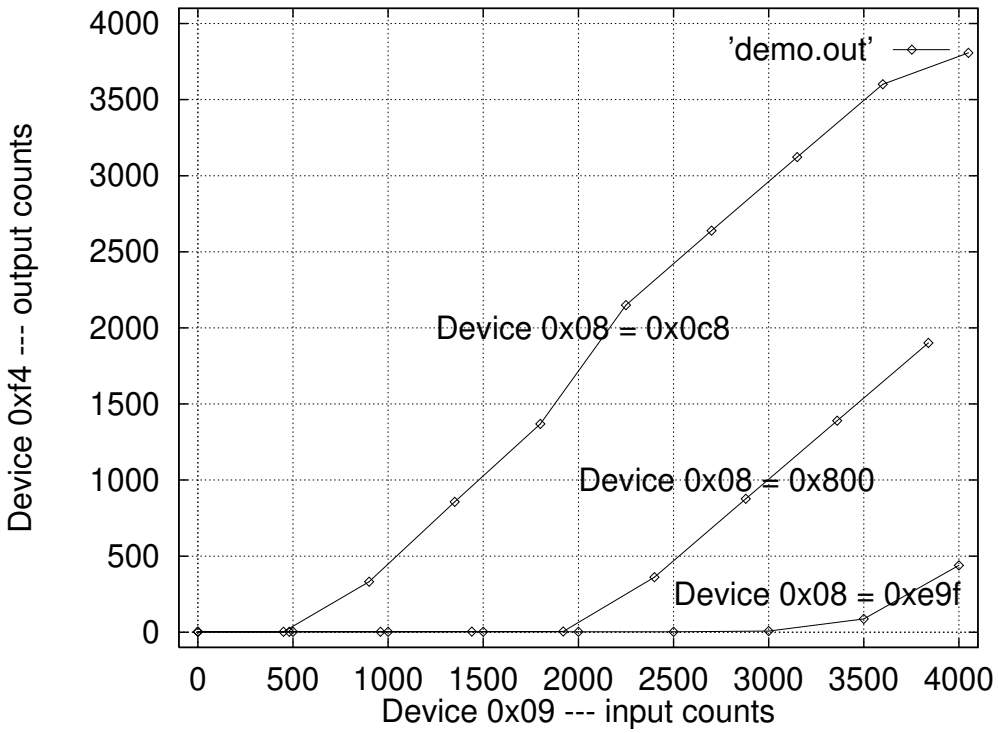

Figure 17: Plotted KLLA response
Test data from Figure 18 are plotted here, using the widely-available `gnuplot` data-plotting program.

Figure 18, next page: "demo.out" is a flat text file. The user ran the 'V' command to set the test-reference voltages (both are connected for positive voltage, but `ftntest` doesn't know that). Then 'w' to set device **0x08**, followed by 'l' to sweep device **0x09** and read device **0xf4**, were run three times to make a set of response curves — three distinct sweep intervals have been chosen. Optional hexadecimal and binary results are also available, in a format suitable for the `gnuplot` plotting program.

```
# Now:  Vss=-10.000, Vdd=10.000.
# DAC $08 gets $e9f  (1110_1001_1111)
# signal: DAC $9;  response: ADC $4
   0     3  #  $  0  $  3  ##  0000_0000_0000  0000_0000_0011
 500     3  #  $1f4  $  3  ##  0001_1111_0100  0000_0000_0011
1000     3  #  $3e8  $  3  ##  0011_1110_1000  0000_0000_0011
1500     3  #  $5dc  $  3  ##  0101_1101_1100  0000_0000_0011
2000     3  #  $7d0  $  3  ##  0111_1101_0000  0000_0000_0011
2500     3  #  $9c4  $  3  ##  1001_1100_0100  0000_0000_0011
3000     7  #  $bb8  $  7  ##  1011_1011_1000  0000_0000_0111
3500    87  #  $dac  $ 57  ##  1101_1010_1100  0000_0101_0111
4000   439  #  $fa0  $1b7  ##  1111_1010_0000  0001_1011_0111

# DAC $08 gets $0c8  (0000_1100_1000)
# signal: DAC $9;  response: ADC $4
   0     3  #  $  0  $  3  ##  0000_0000_0000  0000_0000_0011
 450     3  #  $1c2  $  3  ##  0001_1100_0010  0000_0000_0011
 900   332  #  $384  $14c  ##  0011_1000_0100  0001_0100_1100
1350   856  #  $546  $358  ##  0101_0100_0110  0011_0101_1000
1800  1369  #  $708  $559  ##  0111_0000_1000  0101_0101_1001
2250  2150  #  $8ca  $866  ##  1000_1100_1010  1000_0110_0110
2700  2639  #  $a8c  $a4f  ##  1010_1000_1100  1010_0100_1111
3150  3122  #  $c4e  $c32  ##  1100_0100_1110  1100_0011_0010
3600  3601  #  $e10  $e11  ##  1110_0001_0000  1110_0001_0001
4050  3807  #  $fd2  $edf  ##  1111_1101_0010  1110_1101_1111

# DAC $08 gets $800  (1000_0000_0000)
# signal: DAC $9;  response: ADC $4
   0     3  #  $  0  $  3  ##  0000_0000_0000  0000_0000_0011
 480     3  #  $1e0  $  3  ##  0001_1110_0000  0000_0000_0011
 960     3  #  $3c0  $  3  ##  0011_1100_0000  0000_0000_0011
1440     4  #  $5a0  $  4  ##  0101_1010_0000  0000_0000_0100
1920     5  #  $780  $  5  ##  0111_1000_0000  0000_0000_0101
2400   361  #  $960  $169  ##  1001_0110_0000  0001_0110_1001
2880   877  #  $b40  $36d  ##  1011_0100_0000  0011_0110_1101
3360  1390  #  $d20  $56e  ##  1101_0010_0000  0101_0110_1110
3840  1901  #  $f00  $76d  ##  1111_0000_0000  0111_0110_1101


# 1994 Aug 31, Wed 14:23:23
```

Figure 18: `ftntest`'s Output File

A ATB Control Software

Available separately:

A.1 Library Routines

A.2 `ftntest` Testing Program

A.3 Utility Functions

A.4 Makefile