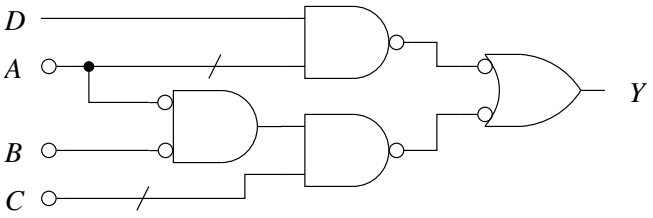
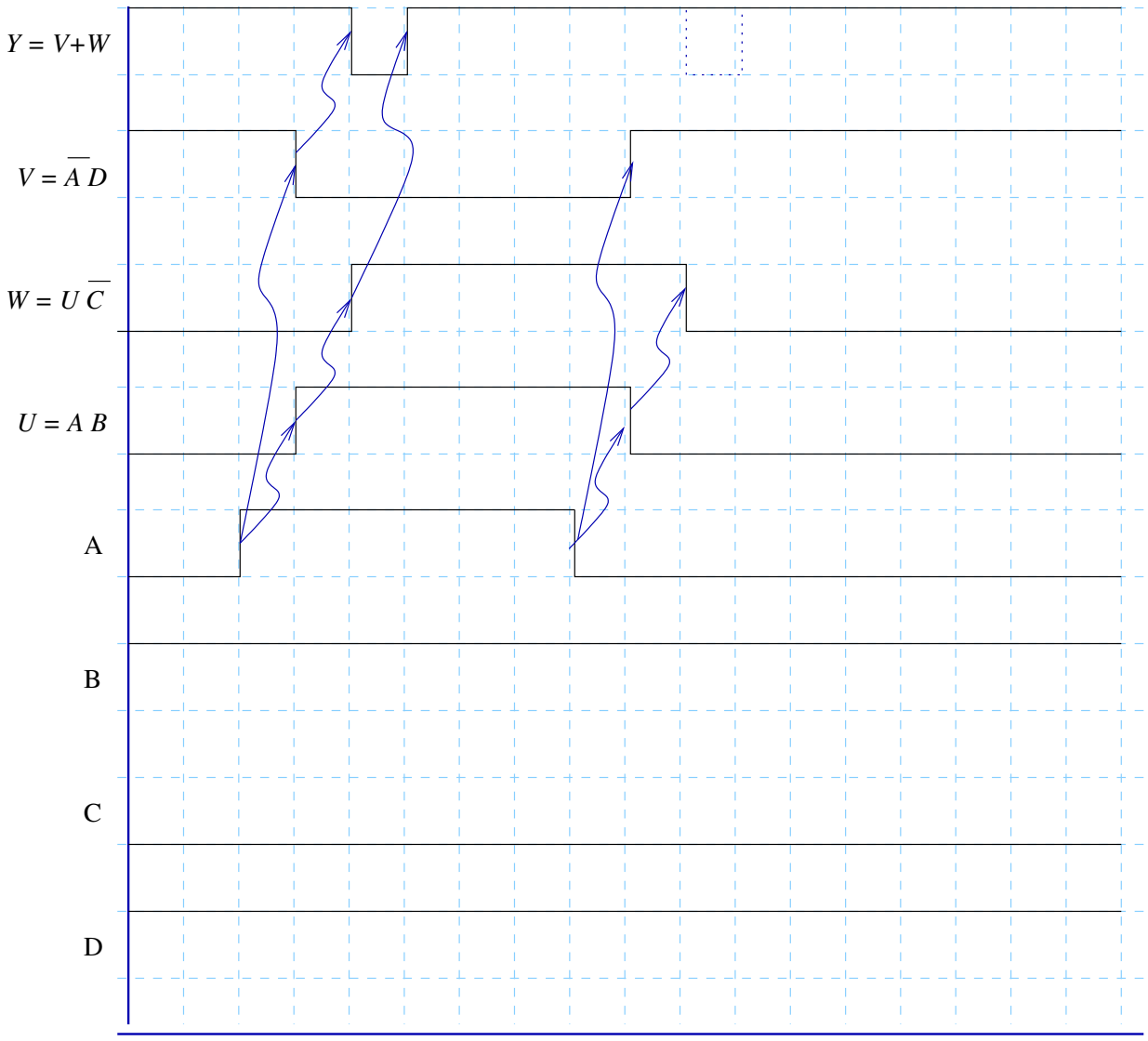
Hazards and Glitches

Consider this implementation (right) of $\overline{A}\,D + A\,B\,\overline{C}$.



glitch a spurious (or illogical) output event due to physical characteristics of the circuit realization.

hazard the potential to produce a *glitch*, which is

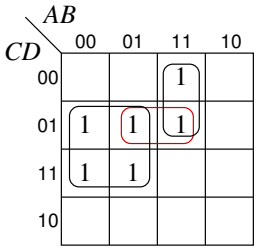


Hazard Analysis

It is extremely difficult to analyze a circuit for hazards. One must consider all relevant input sequences of length k, where k is the longest path from an input to the output. In this example, a thorough analysis might require as many as 3×2^4 scenarios to be considered.

For small conbinational circuits K-maps can be used to identify and mask "basic" hazards As can be seen in this K-map, the minimal SOP has two adjacent cubes that do not overlap, indicating a hazard when $B = 1$, $C = 0$, $D = 1$ and input A changes.

$$\bar{A}D + AB\bar{C}$$



The hazard can be masked by adding a redundant clause, $\overline{A}\,D + A\,B\,\overline{C} + B\,\overline{C}\,D$ "bridging" the gap between the covering cubes.

It remains to determine whether and under what conditions a glitch actually occurs. The cube adjacency gives the hazard condition, $B\,\overline{C}\,D$, so the hazard in this case is associated with a transition on A when $B = D = 1$ and $C = 0$. The question is whether $1\nearrow 0$ transition a $0\searrow 1$ transition, or both, on A result in a glitch. The unit-delay timing analysis above shows that when A changes from 0 to 1 a glitch occurs, but not when A changes from 1 to 0.

In the K-map analysis, an important assumption[1] is that *just one* input changes at any time. Thus, hazards involving simultaneous changes on two inputs are not exposed.

[1] called the *fundamental mode* assumption.